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(54) LIQUID CRYSTAL DISPLAY HAVING A DUAL SHIFT CLOCK WIRE

Abstract

Blackstone Translation

1 In the liquid crystal display, the timing controller producing the image data signal and the shift clock signal for shifting this image data signal is formed in data driver integrated circuit and the other printed circuit board. In the printed circuit board in which the timing controller is formed, it transmits with the first signal wiring for transmitting the shift clock signal and the second signal wiring for being the same frequency as the shift clock signal and transmitting the first clock signal in which a phase is an opposite is formed. In this way, in the second signal wiring of the printed circuit board, because the clock signal having the shift clock signal and anti-phase is transmitted, the electromagnetic interference caused by the shift clock signal electrical transmission is reduced



Fig. 2



The EMI, shift clock signal, dual shift clock wire, timing controller, LCD driving circuit.

Description

- Brief explanation of the drawing

2 Fig. 1 is a drawing showing the conventional thin film transistor liquid crystal display.

- 3 Fig. 2 is a drawing showing the thin film transistor liquid crystal display according to the first preferred embodiment of the present invention.
- 4 Fig. 3 is a vertical side view of the A-A' line of Fig. 2.
- 5 Fig. 4 is a detail block diagram of data driver integrated circuit according to the first preferred embodiment of the present invention.
- 6 Fig. 5 is a drawing showing the waveform of the clock signal according to the first preferred embodiment of the present invention.
- 7 Fig. 6 is a schematical diagram of the thin film transistor liquid crystal display according to the second preferred embodiment of the present invention.
- 8 Fig. 7 is a drawing showing the waveform of the shift clock signal and picture signal according to the second preferred embodiment of the present invention.
- 9 Figs. 8 and Figs. 8 is a drawing showing the waveform of the picture signal according to the third preferred embodiment and shift clock signal.
- 10 Fig. 10 is a drawing showing the waveform of the shift clock signal and picture signal according to the fourth preferred embodiment of the present invention.

Details of the Invention

‣ Purpose of the Invention

The Technical Field to which the Invention Belongs and the Prior Art in that Field

- 11 The present invention relates to the liquid crystal display, particularly, to the liquid crystal display for having the shift clock wire.
- 12 Fig. 1 is a drawing showing the conventional thin film transistor liquid crystal display (thin film transistor liquid display: TFT-LCD).
- 13 As shown in Fig. 1, TFT-LCD is made of generally, the LCD panel (10), data driver (20), and the gate driving and timing controller (30).
- 14 In the LCD panel (10), a plurality of gate lines (not illustrated) which is the scanning line is parallelly formed. A data line (not illustrated) is formed to a plurality of data lines (not illustrated) in which the picture signal is applied to be insulated with the gate lines and intersect. The domain surrounded with a plurality of data lines and gate line forms a pixel. And the thin film transistor (thin film transistor: TFT) which is the switching element is formed in each pixel. In the gate electrode of the TFT, and the source electrode and drain electrode, the respective gate line, and data line and pixel electrode are connected.
- 15 The data driver (20) is electrically connected to data line of the LCD panel (10). And it authorizes R, in which the digital signal outputted from the timing controller (40) G, and B data signal and control signal are input to the data driver (20). And it outputs G, and B data voltage in each data line of the LCD panel (10) to the line unit.
- 16 At this time, because it has the problem that the number of output pin all data lines of the LCD panel are increased to one integrated circuit (integrated circuit: IC), generally data driver (20) is comprised of a plurality of data driver integrated circuits (20a, 20b, 20c, 20d).

17 The gate driving unit (30) is electrically connected to the gate line of the LCD panel. And it successively authorizes the gate on voltage for making coming TFT which is the switching element in the gate line. If TFT connected to or disconnected from the gate on voltage among a plurality of gate lines is turned on, data voltage applied as data line is delivered to the pixel electrode through the drain electrode of TFT. The gate driving unit (30) is made of data driver and register, and is similar of a plurality of gate driver integrated circuits (30a, 30b, 30c, 30d).

18 The timing controller (40) outputs R, G, and B data signal and all kinds of the timing signals to data driver (20) and gate driving unit (30). The timing controller (40) is formed in the printed circuit board (printed circuit board: PCB) separated from data driver (20) and gate driving unit (30). And it transmits all kinds of the timing signals and R, G, B data signal through the wiring formed in this PCB (50) in the outside data driver (20) or the gate driving unit (30).

19 At this time, there can be data signal, which is the high frequency among the transmitted signal and the shift clock signal for storing this picture signal in the shift register (not illustrated) of data driver (20) as data driver (20) from timing controller (40).

20 As to this shift clock signal, the clock frequency for example over 65MHz in case of being the XGA class TFT. And the electromagnetic interference (electro-magnetic interference: EMI) problem occurs in case of transmitting shift clock with all data driver integrated circuits (20a, 20b, 20c, 20d) through the wiring of the PCB (50).

21 Particularly, the PCB (50) of TFT-LCD is nearly the same as that of the length of the longer side of the LCD panel as shown in Fig. 1, it transmits the shift clock signal in moreover, all data driver integrated circuits (20a, 20b, 20c, 20d). Therefore the length of the wiring transmitting the high-speed shift clock is very large. Accordingly, EMI caused by the electrical transmission of the high-speed shift clock consists of especially, a problem in TFT-LCD.

Technical challenges of the Invention

22 An object of the present invention is that a problem as described above is solved. Therefore, EMI caused by the high-speed shift clock signal and data signaling message is to be reduced.

▶ **Structure & Operation of the Invention**

23 The purpose as described above is achieved. And the liquid crystal display according to one feature of the present invention is equipped with the printed circuit board which it has with the panel of liquid crystal display: including a plurality of data lines, a plurality of gate lines intersecting in data line, and a plurality of pixels having the switching element and the gate driving unit which successively authorizes the gate voltage for turning the switching element in a plurality of gate lines and data driver authorizing the gradation voltage showing the image data signal in correspondence to the line unit and the image data signal transmitted in data driver and the timing controller producing the shift clock signal for shifting the image data signal, and the first signal wiring for transmitting the shift clock signal and the second signal wiring for transmitting the first clock signal which is the same frequency as the shift clock signal and has the phase difference of 90° or 270° is formed. A plurality of pixels having the switching element is connected to the gate line and data line while being arranged to the matrix type.

24 Here, it is preferable that the second signal wiring is connected to the earth point through the predetermined resistance value. Moreover, it is preferable that the first clock signal has the phase difference of 180° between the shift clock signal being generated from the timing controller.

25 Moreover, data driver provides the output buffer which the respective image data signal and shift clock signal are transmitted, and it is made of a plurality of data driver integrated circuits authorizing the gradation voltage corresponding to the image data signal in the predetermined data line, and after each data driver integrated circuit receives the shift register which stores while synchronizing in the shift clock signal and shifting the image data.

and the image data signal stored in the shift register and at this time, it temporary-saves the digital-to-analog converter: which changes to the gradation voltage corresponding to the image data signal and the gradation \ outputted from the digital-to-analog converter, authorizes the gradation voltage in response to the load signal predetermined data line to the line unit.

26 In the meantime, the liquid crystal display according to the other feature of the present invention is equipped \ panel of liquid crystal display:, including a plurality of data lines, a plurality of gate lines intersecting in data lin plurality of pixels having the switching element the gate driving unit, which successively authorizes the gate v turning the switching element on in a plurality of gate lines data driver authorizing the gradation voltage showi image data signal in data line to the line unit and the printed circuit board which receives the serially transmitt data signal and producing the first image data signal and the second image data signal from the image data s and in which the respective first for transmitting and the second clock wiring are the respective first for transm the second image signal wiring and the first and the second shift clock signal the timing controller, which prod respective first for shifting and the second shift clock signal the first and the second image signal while having phase difference within 90. or 270. and the first and the second image data signal formed. A plurality of pi having the switching element is connected to the gate line and data line while being arranged to the matrix tyj

28 Here, it is preferable that the first image data signal is the odd numbered signal among the image data signal second image data signal is the even numbered turn signal among the image data signal.

29 Moreover, it is preferable that the thing which the first and the second shift clock signal have the phase differ 180. is desirable. And at this time, the first image data signal and the second image data signal have the ph difference within 90. or 270. range.

30 Hereinafter, referring to the figure, concretely the embodiment of the present invention is illustrated.

31 Fig. 2 is a drawing showing the TFT-LCD according to the first preferred embodiment of the present invention

32 As shown in Fig. 2, the TFT-LCD according to the first preferred embodiment of the present invention is made panel (100), data driver (200), and the gate driving unit (300) and timing controller (550).

33 The LCD panel (100) is made of the TFT substrate (120) and color filter substrate (110), and the liquid crystal injected between a two-board.

34 In the color filter substrate (110), the common electrode (not illustrated) in which the common voltage is appli G, and B color filter layer (not illustrated) are formed.

35 In the TFT substrate (120), a plurality of gate lines (Gn) which is the scanning line is parallelly formed. And it i to a plurality of data lines (Dm) in which the picture signal is applied be insulated with the gate line and intersect domain surrounded with a plurality of data lines and gate line forms the pixel. And the TFT (125) which is the element is formed in each pixel. In the gate electrode of the TFT (125), and the source electrode and drain ele the respective gate line, and data line and pixel electrode are connected. The liquid crystal layer was injected the pixel electrode and common electrode. And this was shown in terms of an equivalent in the liquid crystal c (Cl). Moreover, in the pixel electrode, the maintenance (storage) capacitor (Cst) for maintaining the voltage ct the liquid crystal capacitance is formed.

36 As to data driver (200), a plurality of data driver integrated circuits (200a, 200b, 200c, 200d) and driver IC are the respective adhered tape carrier plate (tape carrier plate: TCP) (250a, 250b, 250c, 250d).

37 In Fig. 2, the respective data driver integrated circuit is adhered on TCPs (250a, 250b, 250c, 250c, 250d). An

signal wire, for connecting the PCB (500) and data driver integrated circuit to this TCP and the signal wire for connecting data pads (127a, 127b, 127c, 127d) formed after each data line of the TFT substrate and data driver integrated circuit are molded. As shown in Fig. 3, this TCP electrically connects the LCD panel and PCB to data driver integrated circuit.

38 Fig. 3 is a drawing showing the vertical side view cut with the A-A' line of Fig. 2.

39 As shown in Fig. 3, the liquid crystal (104) is injected between the TFT substrate (120) and color filter substrate (120). And this liquid crystal is soldered with the sealant (106) formed between a two-board. In the end part of data pad (127a) formed on the TFT substrate (120), data pad (127a) is formed. And the anisotropic conductive film (anisotropic conductive film: ACF) (270a) is formed on this data pad. This ACF (270a) is adhered to the TCP (250a). The data pad (127a) and data driver integrated circuit (200a) are electrically connected. Moreover, the TCP (250a) is connected to the PCB (500) and all kinds of the signals from the timing controller is transmitted to data driver integrated circuit (200a). At this time, as shown in Fig. 3, the TCP (250a) and PCB (500) can be connected through the ACF (270a). And it can be connected through a brazing.

40 As to data driver integrated circuits (200a, 200b, 200c, 200d), the R, G, B data signal, clock signal and the control signal outputted from the respective timing controller (550) are input and it is made of R, G, B, the shift register (210a). The data voltage is authorized in each data line of the TFT substrate (120) to the line unit, and D / A (digital/analog converter (220a) and output buffer (230). R is the analog signal.

41 In Fig. 4, while synchronizing R, transmitted from the timing controller (550) G, and B data in the shift clock (C *** shifting, the shift register (210a) stores. At this time, if data are altogether stored in the shift register of data driver integrated circuit (200a), data driver integrated circuit sends the carry out signal to the next time data driver integrated circuit (220b). The next time data driver integrated circuit (220a) operates like the previous data driver IC.

42 The digital-to-analog converter (220a) changes to the analog gray voltage value corresponding data signal stored in the shift register (210a). That is, the digital-to-analog converter (220a) receives the gradation voltage (V1, V2, V3) outputted from the gradation voltage generation part (not illustrated) and data signal outputted from the shift register (210a). It outputs the analog gray voltage value corresponding to data signal stored in the shift register.

43 When the output buffer (230a) stores the analog gray voltage outputted from the digital-to-analog converter (220a), the load signal (LOAD) signal is applied, it authorizes the analog gray voltage in data line electrically connected to data driver integrated circuit to the line unit.

44 The gate driving unit (300) is electrically connected to the gate line of the TFT substrate (120). And a plurality of gate driver integrated circuits (300a, 300b, 300c, 300d) and driver IC are made of the respective adhered TCPs (350a, 350b, 350c, 350d). Gate driver integrated circuits (300a, 300b, 300c, 300d) electrically connect gate pads (127a, 127b, 127c, 127d) and PCB (400) of the TFT substrate by using TCPs (350a, 350b, 350c, 350d) like data driver integrated circuit.

45 The gate driving unit (300) successively authorizes the gate on voltage for making coming TFT which is the source element in the gate line. If TFT connected to one gate line by the gate on voltage among a plurality of gate lines turned on, data voltage applied as data line is delivered to the pixel electrode through the drain electrode of TFT.

46 The timing controller (550) outputs R, G, and B data signal and all kinds of the timing signals to data driver (200a) and gate driving unit (300). The timing controller (550) is formed in the PCB (500) which is the multilayer board. A timing controller (550) transmits all kinds of the timing signals and R, G, and B data signal through the wiring formed in this PCB (500) outside data driver (200) or the gate driving unit (300).

- 47 The timing controller (550) transmits the shift clock signal (CLK1) with each data driver integrated circuit (200, 200c, 200d). And in order to reduce the EMI problem by the shift clock signal (CLK1), it is the same frequency shown in Fig. 5, as the shift clock signal (CLK1) and it transmits the clock signal (CLK2) in which a phase is an opposite through the resistance (Re) in the ground.
- 48 That is, the clock signal (CLK2) wiring which is a kind of heap (dummy) wiring on the PCB (500) is arranged to parallel to the shift clock signal (CLK1) wiring. The clock signal (CLK2) in which the shift clock signal (CLK1) is phase are an opposite is authorized in this dummy line. In that way EMI hereinafter, as described above, caused the shift clock signal (CLK1) is offset.
- 49 Generally, in TFT-LCD, the EMI problem of being caused by the high frequency signal transmission is initiated which is the multilayer board from a relation with the high-frequency line of the stripline type and the formed ground plane which is adjacent to this line. That is, in the ground plane by the electric field generated between the high frequency line and ground plane, the electric charge having the high-frequency line and opposite polarity is generated. At this time, the size of EMI is in proportion to the change of the current at the ground plane of the electric charge moves.
- 50 Therefore, the current change amount at the ground plane can be minimized. It can minimize the EMI problem.
- 51 The liquid crystal display according to the first preferred embodiment of the present invention transmits the clock signal (CLK2) which is the same frequency as the shift clock signal (CLK1) in consideration of this kind of point and anti-phase through the resistance (Re) in the ground. In this way, when it did, it assumed that (-) electric charge is induced in for example, the ground plane of the transmission line attention of the shift clock signal (CLK1), (+) electric charge is induced in the ground plane of the transmission line attention of the clock signal (CLK2). Therefore, it is offset. It transmits it is induced in the ground plane. Therefore, according to the first preferred embodiment of the present invention, the current of the ground plane corresponding to the shift clock signal can be minimized. Thus the EMI generation can be minimized.
- 52 In the meantime, in the first preferred embodiment of the present invention, the clock signal (CLK2) is outputted the shift clock signal (CLK1) from the timing controller (550). But it can be outputted from the separate IC. Moreover, in the first preferred embodiment of the present invention, the shift clock signal (CLK1) wiring and the clock signal (CLK2) wiring be parallelly arranged and form on the same layer. But thing are desirable it can form on the other layer while nots being certainly thus restricted.
- 53 That is, generally, the multilayer PCB is comprised of the insulating layer between the wiring area of the multi-layer and the wiring area. The shift clock signal (CLK1) wiring and clock signal wiring (CLK2) can form on not only one layer but also the different layer.
- 54 Moreover, in the first preferred embodiment of the present invention, it had the phase of the clock signal CLK2 to the shift clock signal CLK1 to that is, 180°. on the contrary. But besides it has the phase difference of 90° or 270°.
- 55 Next, it illustrates for the second preferred embodiment of the present invention.
- 56 Fig. 6 is a schematical diagram of the liquid crystal display according to the second preferred embodiment of the present invention.
- 57 As shown in Fig. 6, the TFT-LCD according to the second preferred embodiment of the present invention is made of the LCD panel (100), gate driving unit (300), data driver (600), timing controller (750). In the second preferred embodiment of the present invention, it omits the overlapped since the LCD panel (100), and the gate driving unit (300) are identical with the first preferred embodiment shown in Fig. 2 description.

58 As shown in Fig. 6, the timing controller (750) according to the second preferred embodiment of the present invention transmits odd image data applied as the odd data line and the even picture data signal applied as the even data line with data driver integrated circuits (600a, 600b, 600c, 600d) through the separate signal wire (L1, L2). And it transmits the shift clock signal (CLK3, CLK4) which is moreover, this image data signal and synchronizing signal through the signal wire (D1, D2) in data driver integrated circuit.

59 That is, according to the second preferred embodiment of the present invention, the timing controller (750) transmits odd image data and shift clock signal (CLK3) with data driver integrated circuits (200a, 200c) through the signal wire (L1) and signal wire (D1). And it transmits even picture data and shift clock signal (CLK4) with data driver integrated circuits (200b, 200d) through the signal wire (L2) and signal wire (D2).

60 In this way, in the second preferred embodiment of the present invention, image data is the main part and transmits in the respective driver IC. Therefore the frequency of the shift clock signal and image data signal can be reduced in comparison with the first preferred embodiment to 1/2. And accordingly the EMI problem can be reduced.

61 Fig. 7 is a drawing showing the odd number according to the second preferred embodiment of the present invention, the even picture data signal and waveform of the shift clock signal (CLK3, CLK4).

62 As shown in Fig. 7, according to the second preferred embodiment of the present invention, the clock signal CLK3 and CLK4 have the same frequency and anti-phase. And moreover, odd image data and even picture data have the same frequency and anti-phase. At this time, odd image data synchronizes in the rising edge of the shift clock signal CLK3 and it is stored in the shift register of data driver integrated circuits (200a, 200c). And it synchronizes in the falling edge of the shift clock signal (CLK4) and even picture data are stored in the shift register of data driver integrated circuits (200b, 200d).

63 Therefore, according to the second preferred embodiment of the present invention, there can be the function of selecting in other words if it does whether it will do to a negative or not as the function, which data driver integrated circuits can select in other words if it synchronizes in the respective rising edge whether it will synchronize in the falling edge or not that is, the positive or the negative clock triggering.

64 The third of the present invention and the fourth preferred embodiment are to solve this kind of clock triggering problem. Figs. 8 and Figs. 8 is a drawing showing the waveform of the odd number followed with the third preferred embodiment of the present invention and the drawing showing the waveform of the even picture data signal, odd image data signal (CLK3, CLK4) the odd number which Fig. 10 follows with the fourth preferred embodiment of the present invention and even picture data signal and shift clock signal (CLK3, CLK4).

65 As shown in Fig. 8, according to the third preferred embodiment of the present invention, the clock signal CLK3 and CLK4 have the same frequency and anti-phase. And moreover, odd image data and even picture data have the same frequency and anti-phase. At this time, the pulse length of CLK4 and clock signal CLK3 exists within the high level section (in other words, the low signal section) of even picture data and respective odd image data. Therefore odd image data and even picture data synchronize in the rising edge (in other words, the falling edge) of CLK4 and respective clock signal CLK3 and as shown in Fig. 8, it can be stored in the shift register within data driver integrated circuit.

66 Consequently, data driver integrated circuit according to the third preferred embodiment of the present invention does not have the need to have the function which selects whether the need will do to a negative or not in other words, clock triggering to the positive. And it can use data driver integrated circuit having only for example, the clock 1 of the positive.

67 In the meantime, Fig. 9 reduces the pulse length of the shift clock signal shown in Fig. 8 by 1/2. It can improve timing margin of data driver integrated circuit as the thing reducing the pulse length of the shift clock signal.

68 According to the fourth preferred embodiment of the present invention, as shown in Fig. 10, the clock signal C CLK4 have the same frequency and anti-phase. And it has the same frequency but odd image data and even data have the phase difference of 90. on the other hand. According to the fourth preferred embodiment of the present invention, because odd image data and even picture data have the phase difference of 90. , it synchronizes in the rising edge (in other words, the falling edge) of CLK4 and respective clock signal CLK3 and it can be stored in the shift register within data driver integrated circuit.

69 Consequently, it does not have the need to have the function which selects whether the need will do to a negative or not in other words if data driver integrated circuit according to the fourth preferred embodiment of the present invention the clock triggering like the third preferred embodiment to the positive. And data driver integrated circuit having for example, the clock triggering of the positive can be used.

70 In the above, it is illustrated for the embodiment of the present invention. But while the present invention is not restricted to the above-described embodiment, the what is possible with the change like deformation or the thing is *** various. For example, in the second preferred embodiment of the present invention, the phase difference of the clock signal (CLK3, CLK4) gives within 90. not only 180. , or 270. range.

71 Moreover, in the second preferred embodiment, it makes the phase of the shift clock signal (CLK3, CLK4) idle. The clock signal in which each shift clock signal (CLK1, CLK4) and phase are an opposite like the first preferred embodiment is transmitted through the separate signal wire in the earth point.

▶ Effects of the Invention

72 As illustrated in the above, according to the present invention, because of transmitting the clock signal which at the same time, has the clock signal and anti-phase with the high-speed shift clock signal, EMI caused by the signal transmission of the shift clock can be reduced. Moreover, because of transmitting even picture data having in phase and anti-phase of the odd number through the separate signal wire, EMI caused by the high-speed picture data transmission can be reduced.

⌚ Scope of Claims

Claim[1] :

73 The liquid crystal display for including panel of liquid crystal display, the gate driving unit, data driver authorizing gradation voltage showing the image data signal in data line to the line unit, and the printed circuit board which with the image data signal transmitted in data driver and the timing controller producing the shift clock signal for shifting the image data signal, and the first signal wiring for transmitting the shift clock signal and including a plurality of data lines, a plurality of gate lines intersecting in data line, and a plurality of pixels having the switching element, the gate driving unit successively authorizes the gate voltage for turning the switching element on in a plural number of lines; and as to the printed circuit board which it has with the image data signal transmitted in data driver and the second signal wiring for transmitting the first clock signal which is the same frequency as the shift clock signal, the phase difference of 90. or 270. is formed.

Claim[2] :

77 The liquid crystal display of claim 1, wherein the second signal wiring is connected to the earth point through a predetermined resistance value.

Claim[3] :

79 The liquid crystal display of claim 2, wherein the first clock signal is generated from the timing controller.

Claim[4] :

81 The liquid crystal display of claim 2, wherein the printed circuit board has the wiring area of a multilayer; and 1 signal wiring and the second signal wiring are parallelly formed in the same layer.

Claim[5] :

84 The liquid crystal display of claim 2, wherein the printed circuit board has the wiring area of a multilayer; and 1 signal wiring and the second signal wiring are formed in the different layer.

Claim[6] :

87 The liquid crystal display of claim 1, wherein the first clock signal has the phase difference of 180. and shift signal.

Claim[7] :

89 The liquid crystal display for including a plurality of data driver integrated circuits authorizing the gradation voltage of the predetermined data line of claim 6, wherein in data driver, the respective image data signal and shift clock are transmitted; and it corresponds to the image data signal.

Claim[8] :

92 The liquid crystal display for including the shift register, the digital-to-analog converter, and the output buffer circuit, wherein: the data driver integrated circuit synchronizes in the shift clock signal; and it stores while shifting the data signal; the digital-to-analog converter receives the image data signal stored in the shift register; and it changes the gradation voltage corresponding to the image data signal; and the output buffer temporary-saves the gradation voltage outputted from the digital-to-analog converter; and authorizes the gradation voltage in response to the signal in the predetermined data line to the line unit.

Claim[9] :

97 The liquid crystal display for including panel of liquid crystal display, the gate driving unit, data driver authorizing the gradation voltage showing the image data signal in data line to the line unit, the timing controller, and the printed circuit board including a plurality of data lines, a plurality of gate lines intersecting in data line, and a plurality of pixel lines, the switching element, and the gate driving unit successively authorizes the gate voltage for turning the switching element on in a plurality of gate lines; the timing controller receives the serially transmitted image data signal and produces the first image data signal and the second image data signal from the image data signal; and produces the respective first for shifting and the second shift clock signal the first and the second image signal while having the phase difference within 90. or 270. ; and as to the printed circuit board, the respective first for transmitting the second clock wiring are the respective first for transmitting and the second image signal wiring and the first and the second shift clock signal the first and the second image data signal formed.

Claim[10] :

101 The liquid crystal display of claim 9, wherein the first image data signal is the odd numbered signal among the image data signal; and the second image data signal is the even numbered turn signal among the image data signal.

Claim[11] :

103 The liquid crystal display of claim 10, wherein the first and the second shift clock signal have the phase difference of 180. .

Claim[12] :

105 The liquid crystal display of claim 11, wherein the first image data signal and the second image data signal have the phase difference within 90. or 270. range.

Claim[13] :

107 The liquid crystal display of claim 12, wherein the first image data signal and the second image data signal have a phase difference of 180°.

Claim[14] :

109 The liquid crystal display of claim 13, wherein the first image data signal synchronizes in the rising edge of the first shift clock signal and it is shifted; and it synchronizes in the falling edge of the second shift clock signal and so the image data is shifted.

Claim[15] :

111 The liquid crystal display of claim 13, wherein the pulse length of the first and the second shift clock signal has the high of the first and second image data or the low signal section.

Claim[16] :

113 The liquid crystal display of claim 12, wherein the first and the second image data signal have the phase difference of 90° or 270°.